A LOW COST, 3-7 GHz, 1/2 WATT MMIC GaAs AMPLIFIER

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ABSTRACT

A low cost, 3-7 GHz, 1/2 Watt MMIC GaAs amplifier has been successfully designed and tested. The amplifier features small chip size (1.2 mm sq.), high gain (12 ±1.5 dB), high power added efficiency (20%), good RF yield (57%) and high tolerance to process variations. Packaged amplifiers were built with this chip for both the 2-6 GHz and the 5.9-6.4 GHz bands. Saturated output power of 25 dBm was achieved in the 2-6 GHz band, and 27 dBm in the 5.9-6.4 GHz band.

INTRODUCTION

Significant progress in the design of GaAs monolithic amplifiers has occurred over the last several years. Impressive power out per FET periphery, high efficiencies, and multioctave bandwidths have been reported [1]. Most of the previously reported designs, however, have had a relatively large chip area, and have utilized such techniques as via hole grounds, excessively thin chips, selective back etching, or wrap around grounds [2-6]. These special processing steps are not only expensive in themselves, but they reduce both MMIC and MIC yields, which further increases the chip cost. The end result is that the solid state amplifier represents a disproportionate part of the cost of any microwave system. The increasing need for MMIC power amplifiers in disposable military systems and low cost communication systems mandates a reduction in the cost of the power amplifiers.

In this paper, we describe a medium power 3-7 GHz amplifier designed to maximize performance for the lowest cost per chip. Improvements made in the electrical design, the MMIC layout, and the processing technology to achieve these goals are discussed.

CIRCUIT DESCRIPTION

Figure 1 shows the schematic of a two-stage MESFET amplifier with 4 mm output, and 6 mm overall, periphery. The circuit integrates all matching, biasing, bypassing and coupling components. Matching sections were designed with minimal series inductances to minimize the circuit losses.

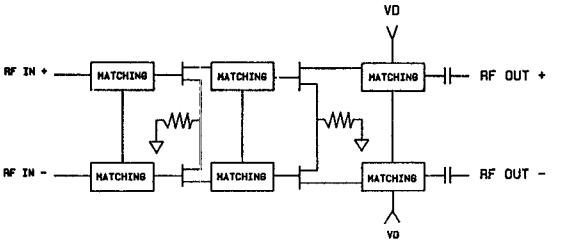

Figure 1. Schematic of the 3-7 GHz MIC Amplifier.

The amplifier uses a novel bias scheme that requires only a single drain supply. The scheme uses a source bias resistor that allows a constant IDS independent of IDSS. Hence, no gate bias correction is needed to achieve the proper FET bias point and the amplifier requires only a single supply. Note that biasing an implanted FET at a constant IDS independent of IDSS also stabilizes the FET reactances - Cgs in particular - which in turn improves RF yields.

The amplifier utilizes a push-pull configuration. This allows the doubling of the output power capability. It also provides for low source impedance and minimum second harmonic distortion.

PROCESSING TECHNOLOGY

The goals in selecting a processing technology were to avoid processing techniques that increase cost and decrease yields, and yet not sacrifice performance. The GaAs power MMIC was manufactured using an ion implanted MESFET process. The virtual ground of the balanced (push-pull) design removes the need for plated through holes (vias). In addition, wafer thinning was not required to establish a ground plane in close proximity to the circuitry. Chip thickness was

determined primarily by thermal considerations. The thickness was selected to be .2 mm, which was sufficient to insure device reliability, yet thick enough to facilitate normal wafer handling. The thickness of the chip was also sufficient to minimize the effects of through capacitances to ground.

Well characterized 1 um FETs were utilized for this design. First metal and air bridge metalizations were used for interconnections. SiN MIMs were used for bypassing and matching capacitors.

LAYOUT

A photomicrograph of the MMIC amplifier is shown in Figure 2. For cost reasons, the amplifier layout was made as compact as possible without sacrificing the chip thermal design. The use of all lumped matching elements facilitated the design compaction. The balanced two-stage amplifier required a 1.2 mm sq. chip area. With this chip size, 3200 MMIC amplifiers can be obtained on a 3" diameter wafer.

For thermal considerations, all heat sources were spread evenly about the chip. The FETs were broken up into 1 mm periphery sections, and then separated at their centers to avoid the central hot spots associated with large periphery power amplifiers. The bias resistors were similarly broken up and spread throughout the chip.

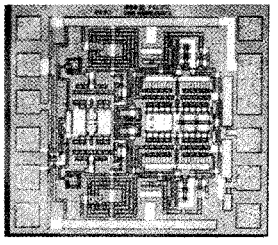

Figure 2. 3-7 GHz MMIC Amplifier Chip Photograph.

Note that power amplifier circuits with their large FET peripheries are particularly sensitive to parasitic source inductances. Very low source inductances can be achieved by the use of a virtual ground as in a push-pull amplifier. This reduction in source inductance makes the amplifier less sensitive to Cgs variations, thereby improving RF yields.

MMIC RESULTS

The performance of the amplifier was first measured at wafer level. Figure 3 is a plot of the small signal gain response of the amplifier. The power amplifier demonstrated 12± 1.5 dB gain across the 3 to 7 GHz band. Figure 4 is a small signal gain plot of all the amplifiers that exhibited a minimum of 10 dB gain. Of the 40 chips on the wafer randomly selected for testing, 23 had at least 10 dB gain for a yield of 57%. For 8 dB minimum gain, the yield would have been 77%. All but 4 devices turned on, for a DC yield of 90%.

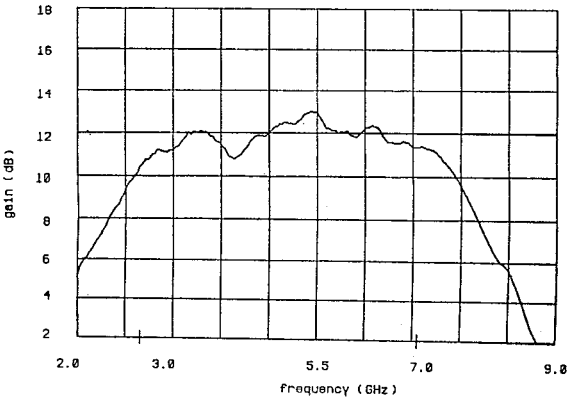

Figure 3. Small Signal Gain vs. Frequency of 3-7 GHz MMIC Amplifier.

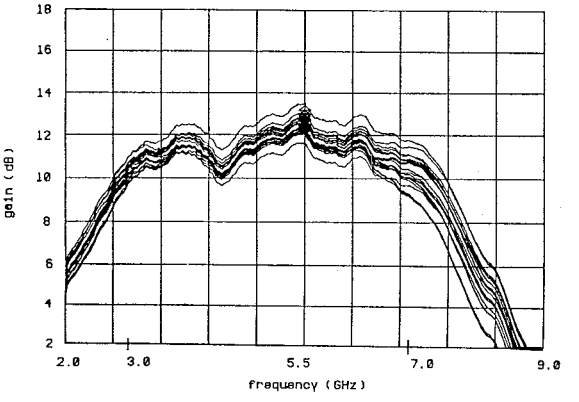

Figure 4. Variation in Gain Across the Wafer for 3-7 GHz MMIC Amplifier.

Figure 5 shows the power saturation characteristics of the amplifier. Saturated power output of 550 mW was achieved across the 3-5.5 GHz band, with an associated gain of 9.5 dB. Using the figure of merit of power out per chip area, this data represents .45 watts/(mm sq.). This, to our knowledge, is the largest power out per chip area reported to this date. At this power level the amplifier dissipates 2.5 Watts, resulting in an overall power added efficiency of 20%.

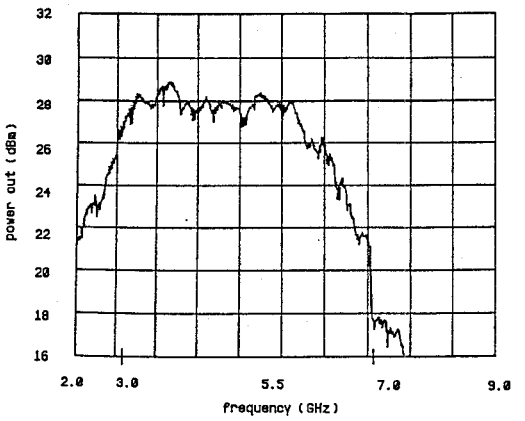

Figure 5. Saturated Power Out of the 3-7 GHz MMIC Amplifier.

PACKAGED MMIC RESULTS

The 1/2 Watt power chip was combined with a 2-6 GHz small signal MMIC amplifier to produce a 2-6 GHz 18 dB gain power amplifier. The low power amplifier was a two-stage push-pull amplifier. It was used to increase the gain of the overall amplifier and to flatten the gain response down to 2 GHz, since the low power amplifier had excess gain at the low end. The combined amplifier also had improved input return loss.

The amplifier was placed in various packages, along with MIC baluns to interface to the unbalanced world. Figure 6a shows the amplifier along with two discrete MIC baluns in a 6-lead package. Figure 6b shows the amplifier on a dual balun BeO substrate in a 4-lead package. Either one of these packages can be used to build multi-stage amplifiers. Both packages provided better than 15 dB return loss up to 8 GHz. Feedback capacitances were kept to a minimum by making the package side walls much higher than the combined MMIC and MIC. Isolation between leads was not an issue in the 4-lead package and was minimized in the 6-lead package by side wall grounds between the leads.

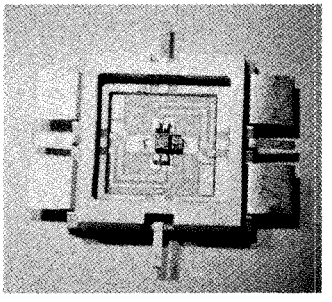

Figure 6a. Two Chip Power Amplifier in 4-Lead Package.

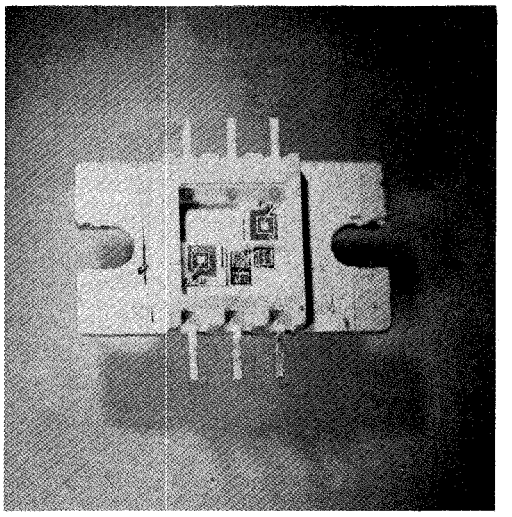

Figure 6b. Two Chip Power Amplifier in 6-Lead Package.

The balun losses in the 2-7 GHz band were typically 1.5 dB. The small signal response of the 6-lead package amplifier is shown in Figure 7.

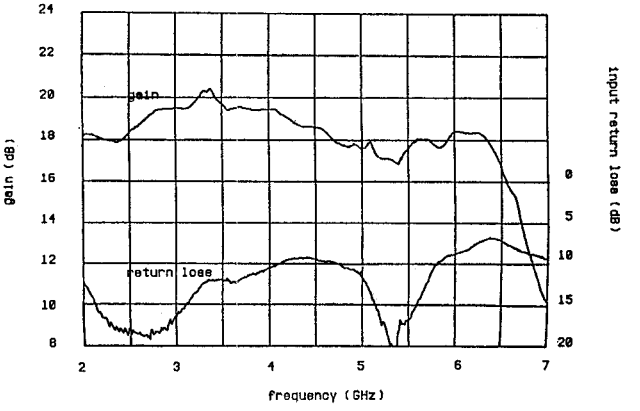

Figure 7. Small Signal Response of 2-6 GHz Packaged Amplifier.

The same amplifier was then inductively tuned using 1 mil bond wires to produce a 1/2 Watt, 5.9-6.4 GHz amplifier. The amplifier had a small signal gain of 18 dB (Figure 8). The saturated response of the amplifier is shown in Figure 9.

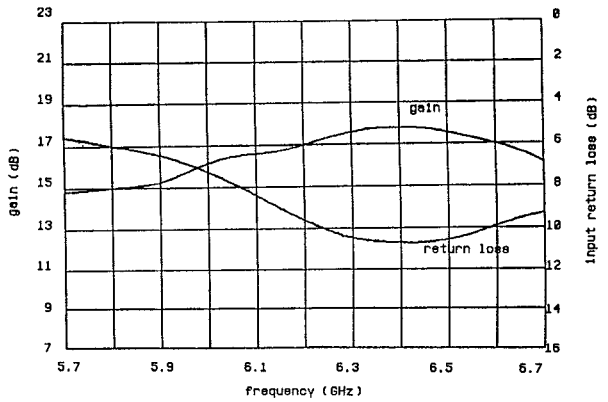

Figure 8. Small Signal Response of 5.9-6.4 GHz Packaged Amplifier.

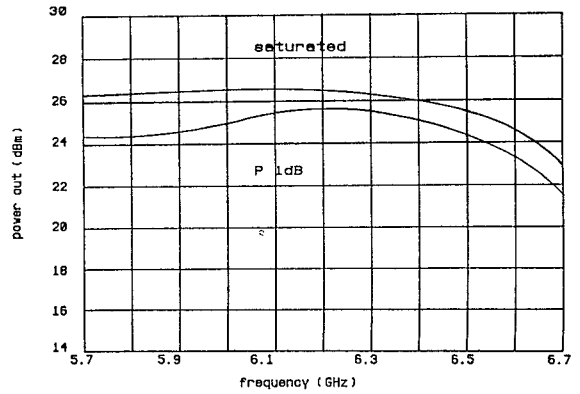

Figure 9. Saturated Response of 5.9-6.4 GHz Packaged Amplifier.

CONCLUSION

GaAs monolithic power amplifiers are entering the age of high RF yields and low cost chips. By paying close attention to processing costs and yield enhancement factors, we developed a 3-7 GHz medium power MMIC amplifier with net overall yields close to 60% on 3" wafers with 3200 possible chips per wafer. The MMIC amplifier was used to make a 2-6 GHz and a 5.9-6.4 GHz packaged amplifier. Both amplifiers typically had 18 dB gain. The narrow band amplifier exhibited a 27 dBm power output.

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